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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/720,564 | 11/24/2003 | Phillip J. Restle | YOR920030455US1 | 5729 |

33233 7590 02/23/2006

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| EXAMINER | |
|---|---|
| LEVIN, NAUM B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/720,564 | RESTLE, PHILLIP J. | |
| | Examiner | Art Unit | |
| | Naum B. Levin | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being unpatentable by Shepard et al. (US Pub. No.: 20050057286).

2. As to claims 1, 8, 12 and 21 Shepard discloses:

(1) An integrated circuit (IC) comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid (The circuit of FIG. 1A illustrates the four sectors 101 being driven by a further clock distribution circuit, such as an H-tree 102, to deliver the clock signal from a master clock 103 to the individual sector driver circuits) having a known load capacitance (the capacitance of the clock distribution circuit can be tuned by including one or more capacitors which can be selectively switched into or out of the clock distribution circuit to optimize the circuit resonance) ([0023]-[0024]; [0033] ;[0037]);

a clock driver driving said clock distribution grid (a clock signal driver coupled to the resonant circuit for driving a clock signal on the clock distribution grid) ([0033]; claim 21);

at least one inductor connected at one end to said distribution grid (the spiral inductors 120 have one end coupled directly to the clock grid 125), said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor (The spiral inductors 120 are formed with a spiral length, spacing and line width to present an inductance value that will substantially resonate with the capacitance presented by the clock tree 115 and clock grid 125 at the desired clock frequency) ([0019]; [0034]; [0036]; claim 9); and

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor (Because the spiral inductors are generally much larger than the power grid, most of the potential deleterious coupling will be to the underlying power grid. To reduce eddy current formation in the underlying grid, the vias in the grid can be dropped and small cuts can be made in the wires. This technique is generally known to those skilled in the art of RF circuit design as it is analogous to ground plane laminations used for spiral inductors in RF circuits) ([0035; [0039).

(8) An integrated circuit (IC) comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid having a known load capacitance ([0023]-[0024]; [0033] ;[0037]);

a clock driver driving a first clock phase in said clock distribution grid (various clock distribution schemes can be used to drive the resonant clock circuit, for example, multiple phase lock loop circuits can be distributed throughout the clock grid with the PLLs driving the grid) ([0033]; [0047]; [0055]; claim 21);

at least one inductor connected at one end to said first clock phase, said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor ([0019]; [0034]; [0036]; claim 9); and

a second clock phase, said at least one inductor being connected to said second phase at an other end, said local grid capacitance comprising local wiring capacitance from both of said first clock phase and said second clock phase ([0019]; [0033]; [0034]; [0036]; [0047]; [0055]; claim 9; claim 21);

(12) An integrated circuit (IC) assembly clocked by a global clock, said global clock being distributed to a plurality of sectors (A typical microprocessor clock distribution may include several dozen of such clock distribution sectors, which are coupled together to provide a global clock distribution circuit- [0033]), each of said sectors comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid (The circuit of FIG. 1A illustrates the four sectors 101 being driven by a further clock distribution circuit, such as an H-tree 102, to deliver the clock signal from a master clock 103 to the individual sector driver circuits) having a known load capacitance (the capacitance of the clock distribution circuit can be tuned by including one or more capacitors which can be selectively switched into or out of the clock distribution circuit to optimize the circuit resonance) ([0023]-[0024]; [0033] ;[0037]);

a clock driver driving said clock distribution grid (a clock signal driver coupled to the resonant circuit for driving a clock signal on the clock distribution grid) ([0033]; claim 21);

at least one inductor connected at one end to said distribution grid (the spiral inductors 120 have one end coupled directly to the clock grid 125), said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor (The spiral inductors 120 are formed with a spiral length, spacing and line width to present an inductance value that will substantially resonate with the capacitance presented by the clock tree 115 and clock grid 125 at the desired clock frequency) ([0019]; [0034]; [0036]; claim 9); and

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor (Because the spiral inductors are generally much larger than the power grid, most of the potential deleterious coupling will be to the underlying power grid. To reduce eddy current formation in the underlying grid, the vias in the grid can be dropped and small cuts can be made in the wires. This technique is generally known to those skilled in the art of RF circuit design as it is analogous to ground plane laminations used for spiral inductors in RF circuits) ([0035; [0039);

(21) An integrated circuit (IC) assembly clocked by a global clock, said global clock being distributed to a plurality of sectors (A typical microprocessor clock distribution may include several dozen of such clock distribution sectors, which are

coupled together to provide a global clock distribution circuit- [0033]), each of said sectors comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid having a known load capacitance ([0023]-[0024]; [0033] ;[0037]);

a clock driver driving a first clock phase in said clock distribution grid (various clock distribution schemes can be used to drive the resonant clock circuit, for example, multiple phase lock loop circuits can be distributed throughout the clock grid with the PLLs driving the grid) ([0033]; [0047]; [0055]; claim 21);

at least one inductor connected at one end to said first clock phase, said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor ([0019]; [0034]; [0036]; claim 9).

3. As to claims 2-7, 9-11, 13-20 and 22-27 Shepard recites:

(2), (13) An IC/assembly, wherein said at least one inductor is connected to a decoupling capacitor (decap) at an other end ([0040]);

(3), (14) An IC/assembly, wherein a voltage develops across each said decap, said voltage being midway between a high level and low level of said clock (mid-rail voltage) ([0034]);

(4), (5), (15), (16) An IC/assembly, wherein a first of said pair being connected between a first supply line and said other end of said inductor and an other of said pair being connected between said other end and a second supply line ([0034]; claim 7);

(6), (23) An IC/assembly, wherein said power grid lines include supply and supply return lines terminating on endpoints ([0039]; [0042]);

(7), (11), (20), (26) An IC/assembly, wherein at least one inductor is four inductors located in four quadrants around said clock driver ([0033]; [0034]; [0043]);

(9), (18), (24) An IC/assembly further comprising a pair of cross coupled inverters ([0012]);

(10), (19), (25) An IC/assembly further comprising a second clock driver driving said second clock phase ([0034]; [0047]; [0055]);

(22) An IC assembly further comprising a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor ([0035; [0039);

(27) An IC assembly, wherein said clock grid is on a first IC chip and ones of said at least one inductor are on an interposer connected to said first chip ([0033]; [0049]-[0051]).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

STACY A. WHITMORE
PRIMARY EXAMINER

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